--Returning now to the embodiment of the invention using the frame 100 of the type shown in Fig. 1, once the epoxy 118 has been placed on the back of the chips as shown in Fig. 6, the assembly comprising the glass substrate 110, the dicing tape 112, and the frame 100, including the chips which been mounted within it, is aligned with a bottom substrate 115. This alignment can be aided by looking through the glass substrate 110 and through via holes 106 to seek alignment with conductively filled vias 117. Such alignment can also be aided by the use of fiduciary marks on the substrate 115 and/or the frame 100 that are to be aligned.--

Please amend paragraph 91 to change substrate "114" to substrate "115" so that it reads as follows:

--In the embodiment shown in Fig. 11 the substrate 115 is a ball grid pad which has a plurality of vias 117 filled with conductive material, and gold plated ball grid pads 119 on its bottom surfaces. Normally the substrate will be a large sheet having a shape and area similar to both the plastic sheet containing the frames 100 and the substrate 110.--

Please amend paragraph 93 to change substrate "114A" to substrate "115A" so that it reads as follows:

--As shown in Fig. 39 a substrate, such as the substrate 115A shown in that figure, can have passive components formed on it before it is joined with the chips 114 and 116. In Fig. 39 these passive components

include a thin film resistor 120 and a thin film capacitor 122.--

Please amend paragraph 94 to change substrate "114" to substrate "115" and to change "fans" to the intended word "tends", so that the paragraph reads as follows:

--Fig. 12 illustrates the assembly after the frame 100 and the chips it is holding have been bonded to the substrate 114. The pressure of the bottom substrate 115 against the epoxy 118 tends to force portions of that epoxy into the gaps between the chips and the frame 100, which helps to further bond those chips in place relative to the frame.--

Please amend paragraph 97 by deleting the text "shown in" from the middle of the word "latex", so the paragraph reads as follows:

--Once the vias 106 have been filled with conductive material and the assembly has been heated to help that epoxy harden and become more conductive, a layer of liquid latex 126 is evenly spread across the top of the assembly. This is done by its spinning, in which centrifugal force is used to spread material across a surface. In some embodiments of the invention, this latex is a self-Vulcanizing latex, such as is sold by Haveatext, Inc.--

Please amend paragraph 98 to replace "epoxy" with the intended word "latex" and to correct a recognition error

with the intended phrase "and the accuracy", so the paragraph reads as follows:

--After the latex 126 has had been hardened, a layer of photoresist 128 is deposited upon it and pattern by photolithographic techniques so as to create gaps 130 in that photoresist which leave portions of the latex surface 128 through which via holes are to be formed uncovered. The bonding pads on the integrated circuits 114 and 116 and via holes 106 over which the via holes are to be made in the latex layer 126 are large enough and far enough apart, and their position is sufficiently exactly known because of the relative rigidity of the frame and the accuracy of the positioning of the integrated circuits, that it is relatively easy to correctly locate via holes over them in the latex layer 126.--

Please amend paragraph 99 to replace mis-recognition error with the intended phrase "in an", so the paragraph reads as follows:

--Once this is been done the assembly shown in Fig. 15 is submitted to a reactive ion etch represented by the vertical arrows 132. A reactive ion etch is one in which chemically reactive ions are rapidly moved back and forth in an oscillating electromagnetic field in a direction generally perpendicular to the surface being etched, so that they will collide with that surface with considerable energy, which enhances their

etching chemical reaction with the material of that surface.--

Please amend paragraph 101 to correct the mis-recognition of the intended word "etch", so the paragraph reads as follows:

--Fig. 16 illustrates the assembly of Fig. 15 after the ion etch has ended, and after the photoresist has been removed. As can be seen from this figure, after this process the latex layer 126 has had holes 134 etched through it in those locations which correspond to the openings 130 in the photoresist shown in Fig. 15. The purpose of these holes is to etch down to the bonding pads of the integrated circuits 114 and 116 and the top of the conductive via holes 106.--

Please amend paragraph 107 to correct two mis-recognition errors, so the paragraph reads as follows:

--In other embodiments of the invention the catalytic particles used are made of any metal in the eighth group on periodic table. This group includes cobalt, palladium, ruthenium, rhodium, platinum, iridium, osmium, nickel, and iron.--

Please amend paragraph 122 to change substrate "114" to substrate "115", so that the paragraph reads as follows:

--In Fig. 29 the assembly of Fig. 28 is flipped upside-down so the chips 114 and 116 can be mounted

upon a substrate 115, which can be of the same types of substrates described above with regard to Fig. 11.--

Please amend paragraph 123 to change substrate "114" to substrate "115, so that the paragraph reads as follows:

--Once the epoxy 118 has had a chance to firmly bond chips 114 and 116 to the substrate 115, the dicing tape 112 is exposed to radiation through the glass 110. This causes the dicing tape to lose its adhesive characteristic, freeing the assembly shown in Fig. 30 from the glass substrate and the dicing tape.---

Please amend paragraph 124 to change latex "126" to latex "126B", change substrate "114" to substrate "115", and change pins "172" to pins "152", so that the paragraph reads as follows:

--Then a layer of liquid latex 126B is placed over the substrate 115 in sufficient thickness to cover the tops of the chips 114 and 116. A third substrate 150 is position so that pins 152 will push via holes into the latex 126B. The surface of the substrate 150 facing the latex and the surface of its pins 152 are covered with Teflon so that they will not stick to the latex.--

Please amend paragraph 125 to change substrate "114" to substrate "115", so that the paragraph reads as follows:

--In Fig. 32 the substrate 150 and its pins 152 are shown pressed against the latex layer 126B so as to flatten out that layer and to cause the pins 152 to extend substantially all the way down to the top surface of the substrate 115.--

Please amend paragraph 126 to change substrate "114" to substrate "115", so that the paragraph reads as follows:

--Once the latex layer 126B has had a chance to cure, the substrate 150 and its pins 152 are removed from the assembly of Fig. 32, leaving the assembly as shown in Fig. 33. In this assembly the top of the latex layer 126B is close to being coplanar with tops of the chips 114 and 116. In addition via holes 106A have been formed in the layers 126B which connect down to the vias 117 contained in the substrate 115.--

Please amend paragraph 129 to change substrate "114" to substrate "115", so that the paragraph reads as follows:

--Fig. 35 illustrates the assembly after the via holes A have been filled with conductive material, such as the conductive epoxy 118 which is also used to attach the chips 114 and 116 to the substrate 115.--

Please amend paragraph 133 to change substrate "114A" to substrate "115A", so that the paragraph reads as follows:

--Fig. 39 is an illustration of a multichip module which is similar to that shown in Fig. 38 except that in its the copper see layers are not separately shown

and the substrate 115A shown in Fig. 39 has had passive components formed on its surface before was attached to the integrated circuits 114 and 116. These components include a thin film resistor 120 and a thin film capacitor 122.--

Please amend paragraph 136 to correct typographical errors, so the paragraph will read as follows:

--The aspects of the present invention relating to the use of metal seed particles to aid in electroless plating are applicable to the plating of metals other than copper. In fact this technique can be used in combination with a deposition of almost any metal which can be deposited by electroless plating. In aspects of the invention which use both a dielectric material and a conductive layer made of material which are relatively flexible, the combination of latex dielectric and a copper conductive layer is a relatively beneficial want because both materials are relatively flexible, and copper is an extremely good conductor.--

IN THE CLAIMS

Please cancel claims 1 through 10 and 23 through 44.

Please amend claim 11 as follows:

-11. (Amended) An electrical circuit comprised of: